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Syed Kamran Haider

Research Interests

Computer Architecture, Multicore Architecture and Modeling, Cache Coherence Protocols, Parallel Programming, Hardware Security, and Performance Analysis.

Education

Jan'14–Jun'17 (Expected) **Ph.D. Electrical and Computer Engineering**
University of Connecticut, Storrs, CT, USA
Advisor: Marten van Dijk
Relevant Coursework: Advanced Multicore Architecture, Information Security

Aug'11–Dec'14 **Master in Embedded Computing Systems**
Norwegian University of Science & Technology (NTNU), Trondheim, Norway
University of Kaiserslautern (TU-KL), Kaiserslautern, Germany
Thesis: An Area Efficient FPGA Implementation of a Reed-Solomon Soft Decoder
Relevant Coursework: Computer Architecture, Embedded Systems Design, Real-time Systems, High Performance Computing with General Purpose GPUs

Sep'07–Jul'11 **B.E. Electronics Engineering**
National University of Sciences and Technology (NUST), Pakistan
Thesis: Development of Electrical Interface of a Tele-Surgical Robot
Relevant Coursework: Computer Architecture, Digital Systems, Operating Systems, VLSI

Experience

Professional

Jun–Aug '15 **Research Intern** *Microsoft Research, Cambridge, UK*
Designed & implemented Lease/Release: an architectural support mechanism for scaling of highly contended data structures and applications.

Jun–Aug '12 **Summer Intern** *Silicon Labs (formerly Energy Micro), Oslo, Norway*
Developed test cases to verify Energy Friendly Radios and Energy Friendly Microcontrollers.

Academic

Fall '15 **Teaching Assistant** *Dept. of ECE, University of Connecticut, Storrs, CT*
ECE3411: Microprocessors Application Laboratory

Jan'14–present **Research Assistant** *Dept. of ECE, University of Connecticut, Storrs, CT*

Research Projects

Secure Processor Architectures
- Designed, in collaboration with MIT, a dynamic prefetcher for Oblivious RAM (ORAM) making it more efficient for secure general purpose computing.
- Explored how capability systems and memory integrity verification schemes can be efficiently implemented together in processor architectures to verify correct execution of programs.
- Ongoing work on exploring new inherently efficient Oblivious RAM constructions.

Efficient Shared-Memory Multicores

- Developed Lease/Release, an extension to standard directory-based cache coherence protocols that allows the cores to lease cache lines, for a short, bounded period of time, resulting in higher scalability under contention.
- Ongoing work on exploring new hardware-software co-deign mechanisms for transactional memory support on top of modern cache coherence protocols.

Hardware Trojan Detection

- Introduced a formal classification of trigger activated hardware Trojans which represents a vast landscape of possible Trojan designs beyond the publicly known state of the art Trojans.
- Designed and implemented HaTCh, a pre-silicon logic testing based algorithm which detects any hardware Trojan from the above mentioned classification with overwhelming probability.

Technical Skills

- *Programming & Scripting:* C, C++, x86/MIPS Assembly, Python, CUDA
- *Hardware Modeling:* Verilog HDL, VHDL
- *Tools:* Xilinx ISE, ModelSim, Proteus, AVR Studio IDE, Matlab, Git, SVN, Latex
- *Others:* Graphite Multicore Simulator, Pthread Library, Intel Pin

Publications

PPoPP '16 **S. K. Haider**, W. Hasenplaugh, D. Alistarh, Lease/Release: Architectural Support for Scaling Contended Data Structures, *Principles & Practice of Parallel Programming, (PPoPP)*, 2016.

MELECON '16 S. Scholl, **S. K. Haider**, N. Wehn, An Efficient Soft Decision Reed-Solomon Decoder for Moderate Throughput, *18th IEEE Mediterranean Electrotechnical Conference (MELECON)*, 2016.

ICCD '15 **S. K. Haider**, M. Ahmad, F. Hijaz, A. Patni, E. Johnson, M. Seita, O. Khan, M. van Dijk, M-MAP: Multi-Factor Memory Authentication for Secure Embedded Processors, *33rd IEEE Int. Conference on Computer Design, (ICCD)*, 2015.

ISCA '15 X. Yu, **S. K. Haider**, L. Ren, C. Fletcher, A. Kwon, M. van Dijk, S. Devadas, PrORAM: Dynamic Prefetcher for Oblivious RAM, *42nd International Symposium on Computer Architecture (ISCA)*, 2015.

HASP '15 M. Ahmad, **S. K. Haider**, F. Hijaz, M. van Dijk, O. Khan, Exploring the Performance Implications of Memory Safety Primitives in Many-core Processors Executing Multi-threaded Workloads, *4th Workshop on Hardware and Architectural Support for Security and Privacy, (HASP)*, 2015.

HCII'15 V. Grindle, **S. K. Haider**, J. Magee, M. van Dijk, Virtual Fingerprint: Image-Based Authentication Increases Privacy for Users of Mouse-Replacement Interfaces, *International Conference on Human-Computer Interaction (HCII)*, 2015.

ePrint IACR '14 **S. K. Haider**, C. Jin, M. Ahmad, D. M. Shila, O. Khan, M. van Dijk, HaTCh: A Formal Framework of Hardware Trojan Design and Detection, *Cryptology ePrint Archive, Report 2014/943,* `eprint.iacr.org/2014/943/`, 2014.

Honors & Awards

'16 Pre-Doctoral Fellowship for Graduate Students ECE Dept., University of Connecticut

'11–'13 Erasmus Mundus Scholarship holder from the European Union

'11 Gold Medalist for Best Academics in undergraduate

'07–'11 Merit Based Scholarship holder during undergraduate

Volunteer

Organized Blood Donation Campaign for Fatimid Foundation at NUST

Worked at Project E-Village to teach basic computer skills to the villagers of Pakistan